6ED003L06-F

Integrated 3 Phase Gate Driver

Power Management & Drives

Never stop thinking

6ED003L06-F

Revision History:	**2008-07**	Rev. 2
Previous Version:	1.8	
Page	Subjects (major changes since last revision)	
8-12	finalized ratings and electrical characteristics	
13	updated short pulse suppression diagram	

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Table of Contents:

6ED003L06-F (preliminary data sheet)

3-PHASE BRIDGE DRIVER IGBT/MOS

1 Overview

1.1 Features

PG-DSO28-17

- Thin-film-SOI-technology
- Insensitivity of the bridge output to negative transient voltages up to -50V given by SOI-technology
- Maximum blocking voltage +600V
- Power supply of the high side drivers via boot strap
- Separate control circuits for all six drivers
- CMOS and LSTTL compatible input (negative logic)
- Signal interlocking of every phase to prevent cross-conduction
- Detection of over-current and under-voltage supply
- 'shut down' of all switches during error conditions
- externally programmable delay for fault clear after over current detection

1.2 Description

The device 6ED003L06-F is a full bridge driver to control power devices like MOS-transistors or IGBTs in 3-phase systems with a maximum blocking voltage of +600V. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch up may occur at all temperature and voltage conditions.

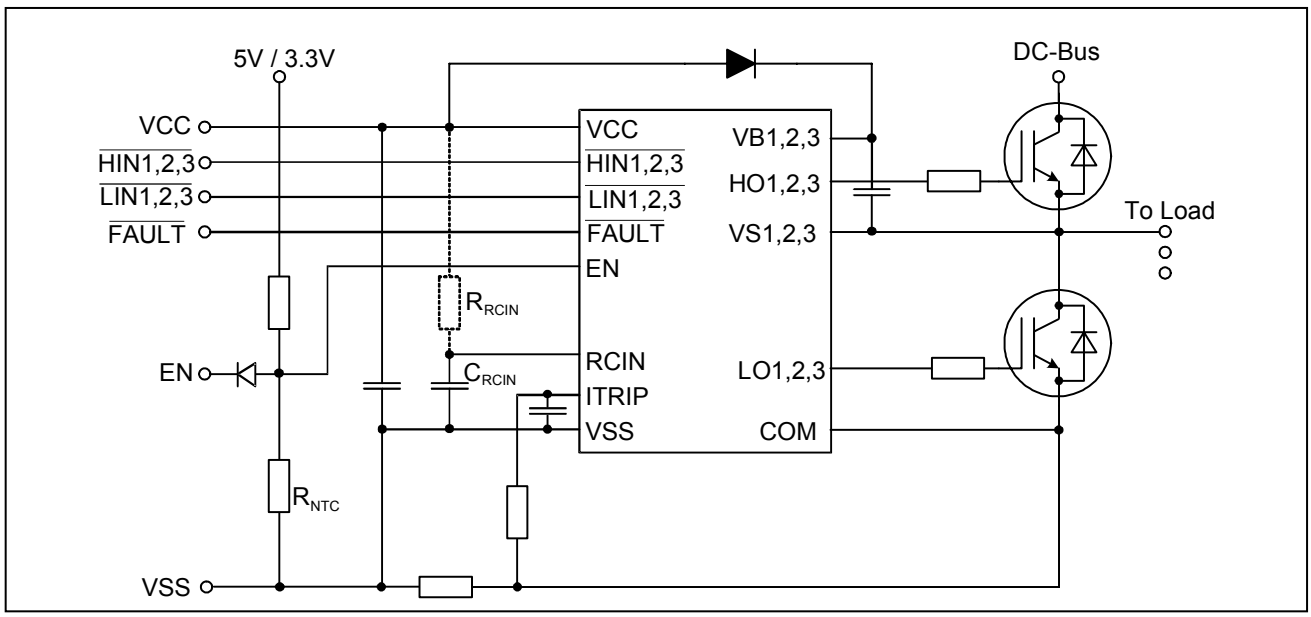


Figure 1: Typical Application

The six independent drivers are controlled at the low-side using CMOS resp. LSTTL compatible signals, down to 3.3V logic. The device includes an under-voltage detection unit with hysterese characteristic and an over-current detection. The over-current level is adjusted by choosing the resistor value and the threshold level at pin ITRIP. Both error conditions (under-voltage and over-current) lead to a definite shut-down off all six switches. An error signal is provided at the FAULT open drain output pin. The blocking time after over-current can be adjusted with an RC-network at pin RCIN. The input RCIN owns an internal current source of 2.8 µA. Therefore, the resistor R_{RCIN} is optional. The minimum output current can be given with 120mA for pull-

up and 250mA for pull down. Because of system safety reasons a 380ns interlocking time has been realised. The function of input EN can optionally be extended with an over-temperature detection, using an external NTC-resistor (see Fig.1). There are parasitic diode structures between pins VCC and VBx due to the monolithic setup of the IC, but external bootstrap diodes are still mandatory.

2 Pin Configuration and Description

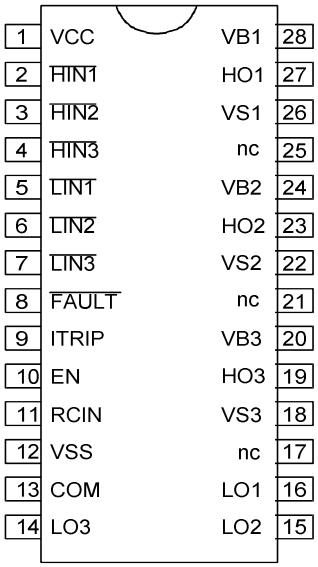


Figure 2: Pin Configuration of 6ED003L06-F

Table 1: Pin Description

Symbol	Description
VCC	Low side power supply
VSS	Logic ground
/HIN1,2,3	High side logic input (negative logic)
/LIN1,2,3	Low side logic input (negative logic)
/FAULT	Indicates over-current and under-voltage (negative logic, open-drain output)
EN	Enable I/O functionality (positive logic)
ITRIP	Analog input for over-current shutdown, activates FAULT and RCIN to VSS
RCIN	external RC-network to define FAULT clear delay after FAULT-Signal (T_{FLTCLR})
COM	Low side gate driver reference
VB1,2,3	High side positive power supply
HO1,2,3	High side gate driver output
VS1,2,3	High side negative power supply
LO1,2,3	Low side gate driver output
nc	Not Connected

2.1 Description

2.1.1 /HIN1,2,3 and /LIN1,2,3 (Low side and high side control pins, Pin 2, 3, 4, 5, 6, 7)

These pins are active low and they are responsible for HO1,2,3 and LO1,2,3 out-of-phase commutation. The schmitt-trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs.

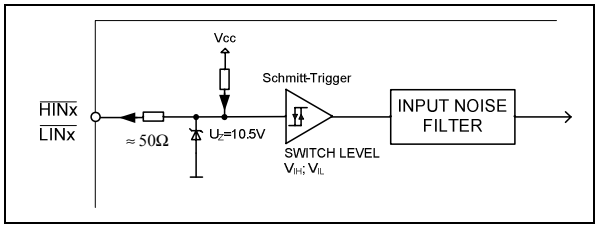


Figure 3: Input pin structure

An internal pull-up resistor of about 75 kΩ is pre-biases the input during supply start-up and a zener clamp is provided for pin protection purposes. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 4 and Figure 7.

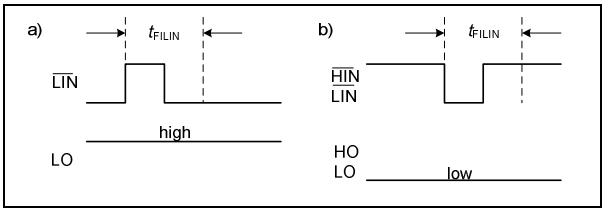


Figure 4: Input filter timing diagram

It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 1us.

The 6ED003L06-F provides additionally an anti-shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only one leg output is activated, so that the leg is kept steadily in a safe state. Please refer to the application note AN-Gatedrive-6ED003L06-1 for a detailed description.

A minimum deadtime insertion of typ 380ns is also provided, in order to reduce cross-conduction of the external power switches.

2.1.2 EN (Gate driver enable, Pin 10)

The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. The internal structure of the pin is the same as Figure 3 made exception of the switching levels of the Schmitt-Trigger, which are here $V_{EN,TH+}$ = 2.1 V and $V_{EN,TH-}$ = 1.3 V. The typical propagation delay time is t_{EN} = 780 ns.

2.1.3 /FAULT (Fault feedback, Pin 8)

/Fault pin is an active low open-drain output indicating the status of the gate driver (see Figure 3). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VCC supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VCC pin description for more details).
- Over-current detection (ITRIP): The fault condition is latched until current trip condition is finished and RCIN input is released (please refer to ITRIP pin).

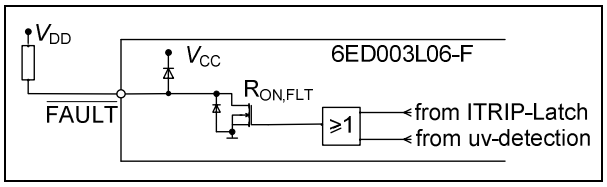


Figure 5: /Fault pin structure

2.1.4 ITRIP and RCIN (Over-current detection function, Pin 9, 11)

6ED003L06-F provides an over-current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ 0.46V) is referenced to VSS ground. A input noise filter (typ: $t_{ITRIPMIN}$ = 210 ns) prevents the driver to detect false over-current events.

Over-current detection generates a hard shut down of all outputs of the gate driver and provides a latched fault feedback at /FAULT pin.

RCIN input/output pin is used to determine the reset time of the fault condition. As soon as ITRIP threshold is exceeded the external capacitor connected to RCIN is fully discharged. The capacitor is then recharged by the RCIN current generator when the over-current condition is finished. As soon as RCIN voltage exceeds the rising threshold of typ $V_{RCIN,TH}$ = 6.0V, the fault condition releases and the driver returns operational following /HIN and /LIN inputs. Please refer to AN-GateDriver-6ED003L06-1 for details on setting RCIN time constant.

2.1.5 VCC, VSS and COM (Low side supply, Pin 1, 12,13)

VCC is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit. Output

power stage is referenced to COM ground.COM ground is floating respect to VSS ground with a recommended range of operation of +/-2.5V. A back-to-back zener structure protects grounds from noise spikes.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage V_{CCUV+} = 12 V is present.

The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below V_{CCUV-} = 10.4 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

2.1.6 VB1,2,3 and VS1,2,3 (High side supplies, Pin 18, 20, 22, 24, 26, 28)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage.

Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VCC.

Under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 12 V and a falling threshold of V_{CCUV-} = 10.4 V. Please refer to Figure 11 of the datasheet for device operating area as a function of the supply voltage. Details on bootstrap supply section and transient immunity can be found in application note AN-GateDriver-6ED003L06-1.

2.1.7 LO1,2,3 and HO1,2,3 (Low and High side outputs, Pin 14, 15, 16, 19, 23, 27)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive of IGBT and MOSFET devices. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs (/LIN1,2,3), while high side outputs (i.e. HO1,2,3) are edge triggered by the respective inputs (/HIN1,2,3). In particular, after an under-voltage condition of the VBS supply, a falling /HIN edge is necessary to turn-on the respective high side output, while after a under-voltage condition of the VCC supply, the low side outputs switch to the state of their respective inputs.

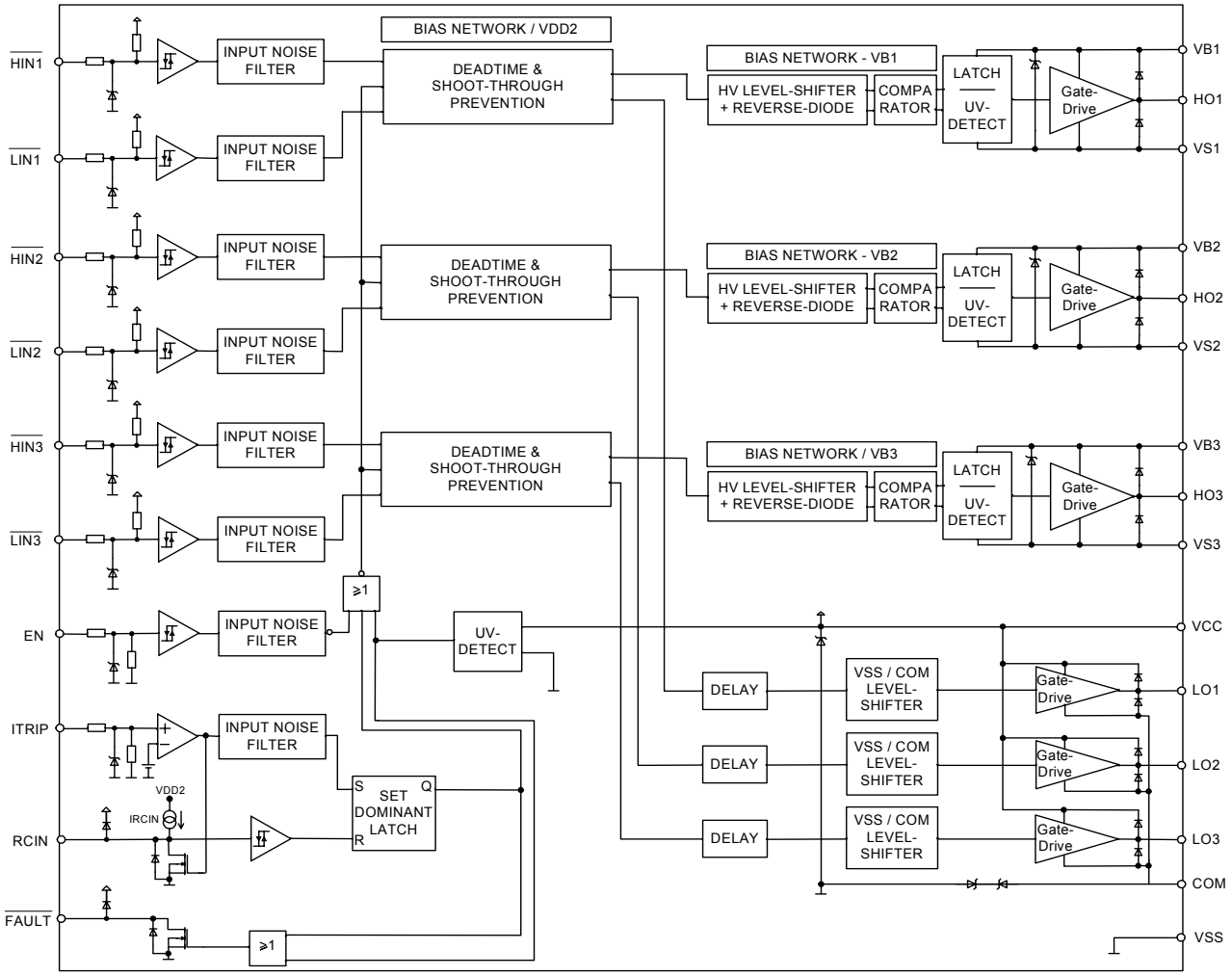


Figure 6: Block diagram

3 Electrical parameters

3.1 Absolute Maximum Ratings

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Max.	Unit
V_S	High side offset voltage(Note 1)	V_{CC}-V_{BS}-6	600	V
	High side offset voltage (t_p<500ns, Note 1)	V_{CC} -V_{BS} -50	-	
V_B	High side offset voltage(Note 1)	V_{CC} - 6	620	
	High side offset voltage (t_p<500ns, Note 1)	V_{CC} - 50	-	
V_{BS}	High side floating supply voltage (V_B vs. V_S)	-1	20	
V_{HO}	High side output voltage (V_{HO} vs. V_S)	-0.5	V_B + 0.5	
V_{CC}	Low side supply voltage (internally clamped)	-1	20	
V_{CCOM}	Low side supply voltage (V_{CC} vs. V_{COM})	-0.5	25	
V_{COM}	Gate driver ground	-5.7	5.7	
V_{LO}	Low side output voltage (V_{LO} vs. V_{COM})	-0.5	V_{CCOM} +0.5	
V_{IN}	Input voltage LIN,HIN,EN,ITRIP t_p <10µs	-1.0	10 15	
V_{FLT}	FAULT output voltage	-0.5	V_{CC} + 0.5	
V_{RCIN}	RCIN output voltage	-0.5	V_{CC} + 0.5	
P_D	Power dissipation (to package) Note 2	-	1.0	W
R_{thJA}	Thermal resistance (junction to ambient, device mounted on PCB see Fig.3)	-	70	K/W
T_J	Junction temperature	-	125	°C
T_S	Storage temperature	-40	150	
d*Vs*/dt	offset voltage slew rate		50	V/ns

Note :The minimal value for ESD immunity is 1.0kV (Human Body Model). ESD immunity inside pins connected to the low side (VCC, HINx, LINx, FAULT, EN, RCIN, ITRIP, VSS, COM, LOx) and pins connected inside each high side itself (VBx, HOx, VSx) is guaranteed up to 1.5kV (Human Body Model).

Note 1 : Insensitivity of bridge output to negative transient voltage up to –50V is not subject to production test – verified by design / characterization. External bootstrap diode is mandatory. Refer to application note.

Note 2: Consistent power dissipation of all outputs

3.2 Required Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Max.	Unit
V_B	High side offset voltage (Note 1)	11.1	620	V
V_{CCOM}	Low side supply voltage (V_{CC} vs. V_{COM})	10	25	

Note 1 : Logic operational for V_B (V_B vs. V_{SS}) > 11,1V

3.3 Operating Range

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Max.	Unit
V_S	High side floating supply offset voltage	V_{CC} -V_{BS}-0.5	550	V
V_{BCC}	High side floating supply offset voltage (V_B vs. V_{CC}, statically, Note 1, Note 2)	-0.5	550	
V_{BS}	High side floating supply voltage (V_B vs. V_S)	13	17.5	
V_{HO}	High side output voltage (V_{HO} vs. V_S)	0	V_{BS}	
V_{LO}	Low side output voltage (V_{LO} vs. V_{COM})	0	20	
V_{CC}	Low side supply voltage	13	17.5	
V_{COM}	Low side ground voltage	-2.5	2.5	
V_{IN}	Logic input voltages LIN,HIN,EN,ITRIP	0	5	
V_{FLT}	FAULT output voltage	0	V_{CC}	
V_{RCIN}	RCIN input voltage	0	V_{CC}	
t_{IN}	Pulse width for ON or OFF (Note 3)	1	-	µs
T_A	Ambient temperature	-40	95	°C

Note 2 : All input pins (/HINx, /LINx) and EN, ITRIP pin are internally clamped with a 10.5V zener diode.

Note 3 : In case of input pulse width at /LINx and /HINx below 1µ the input pulse can not be transmitted properly

3.4 Static Logic function Table

VCC	VBS	RCIN	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
$<V_{CCUV-}$	X	X	X	X	0	0	0
15V	$<V_{BSUV-}$	X	0V	5V	High imp	/LIN1,2,3	0
15V	15V	< 3.3V ↓	0V	5V	0	0	0
15V	15V	X	$> V_{IT,TH+}$	5V	0	0	0
15V	15V	> 5.8V	0V	5V	High imp	/LIN1,2,3	/HIN1,2,3
15V	15V	> 5.8V	0V	0V	High imp	0	0

3.5 Static Parameters

V_{CC} = V_{BS} = 15V unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Logic "0" input voltage (LIN,HIN)	1.7	2.1	2.4	V	
V_{IL}	Logic "1" input voltage (LIN,HIN)	0.7	0.9	1.1		
$V_{EN,TH+}$	EN positive going threshold	1.9	2.1	2.3		
$V_{EN,TH-}$	EN negative going threshold	1.1	1.3	1.5		
$V_{IT,TH+}$	ITRIP positive going threshold	360	460	540	mV	
$V_{IT,HYS}$	ITRIP input hysteresis	60	70			
$V_{RCIN,TH}$	RCIN positive going threshold	-	6.0	7.5	V	
$V_{RCIN,HYS}$	RCIN input hysteresis	-	2.5	-		
V_{OH}	Output voltage (high level, V_{CC}-V_O or V_{BS}-V_O)	-	0.8	1.4		I_O = 20mA
V_{OL}	Output voltage (low level, V_O-V_{COM} or V_O-V_S)	-	0.2	0.6		I_O = -20mA
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	11.0	12	12.8		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	9.5	10.4	11.0		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis	1.2	1.6	-		
I_{LVS+}	High side leakage current betw. VS and VSS	-	1	5	µA	V_S = 600V
I_{LVS+}[1]	High side leakage current betw. VS and VSS	-	30	-	µA	T_j=125°C, V_S = 600V
I_{LVS-}[1]	High side leakage current between VSx and VSy (x=1,2,3 and y=1,2,3)	-	30	-		T_j=125°C V_{Sx} - V_{Sy} =600V

[1] Not subject of production test, verified by characterisation

Symbol	Definition	Min.	Typ.	Max.	Unit	Test Conditions
I_{QBS1}	Quiescent V_{BS} supply current (VB only)	-	300	500		HO=low
I_{QBS2}	Quiescent V_{BS} supply current (VB only)	-	360	550		HO=high
I_{QCC1}	Quiescent V_{CC} supply current (VCC only)	-	0.6	1	mA	V_{LIN}=float.
I_{QCC2}	Quiescent V_{CC} supply current (VCC only)	-	1.1	1.6	mA	V_{LIN}=0V, V_{HIN}=5V,
I_{QCC3}	Quiescent V_{CC} supply current (VCC only)	-	0.9	1.6	mA	V_{LIN}=5V, V_{HIN}=0V
$V_{IN,CLAMP}$	Input clamp voltage (/HIN, /LIN, EN, ITRIP) (Note 1)	9.0	10.6	13	V	I_{IN}=4mA
I_{LIN+}	Input bias current	-	52	100	µA	V_{LIN}=5V
I_{LIN-}	Input bias current	-	110	200		V_{LIN}=0V
I_{HIN+}	Input bias current	-	52	100		V_{HIN}=5V
I_{HIN-}	Input bias current	-	110	200		V_{HIN}=0V
I_{ITRIP+}	Input bias current (ITRIP=high)		70	120		V_{ITRIP}=5V
I_{EN+}	Input bias current (EN=high)	-	69	120		V_{ENABLE}=5V
I_{RCIN}	Input bias current RCIN (internal current source)		2.8			V_{RCIN} = 2 V
I_{O+}	Mean output current for load capacity charging in range from 3V(20%) to 6V(40%)	120	142	-	mA	C_L=10nF
I_{O-}	Mean output current for load capacity discharging in range from 12V(80%) to 9V(60%)	250	410	-		C_L=10nF
$R_{ON,RCIN}$	RCIN low on resistance of the pull down transistors	-	47	100	Ω	V_{RCIN}=0.5V
$R_{ON,FLT}$	FAULT low on resistance of the pull down transistors	-	54	100		V_{FAULT}=0.5V

Note 1: There is an additional power dissipation for input voltages above the clamping voltage. In series to clamping diode there is a limiting resistor of 55Ω (see also Fig.3)

3.6 Dynamic Parameters

V_{CC} = V_{BS} =15V, V_S = V_{SS} = V_{COM}, unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit	Test Condition
t_{on}	Turn-on propagation delay	400	620	800	ns	$V_{LIN/HIN}$=0V
t_{off}	Turn-off propagation delay	400	610	800		$V_{LIN/HIN}$=5V
t_r	Turn-on rise time (CL=1nF)	-	76	130		$V_{LIN/HIN}$=0V
t_f	Turn-off fall time (CL=1nF)	-	26	45		$V_{LIN/HIN}$=5V
t_{EN}	Shutdown propagation delay ENABLE	-	780	1000		V_{EN}=0
t_{ITRIP}	Shutdown propagation delay ITRIP	400	765	1000		V_{ITRIP}=1V
$t_{ITRIPMIN}$	Input filter time ITRIP	155	210	380		
t_{FLT}	Propagation delay ITRIP to FAULT	-	450	700		
t_{FILIN}	Input filter time at LIN for turn on and off and input filter time at HIN for turn on only	120	270	-		$V_{LIN/HIN}$=0V& 5V
t_{FILIN1}	Input filter time at HIN for turn off (Note 1)	100	220	-		V_{HIN} = 5V
t_{FILIN2}	Input filter time at HIN for turn off (Note 1)	-	400	-		V_{HIN} = 5V
t_{FILEN}	Input filter time EN	300	485	-		
t_{FLTCLR}	Fault clear time at RCIN after ITRIP-fault, (CRCin=1nF)	1.0	2.3	3.0	ms	$V_{LIN/HIN}$ = 0 & 5V V_{ITRIP}=0V
DT	Dead time	150	380	-	ns	$V_{LIN/HIN}$ = 0 & 5V
MT_{ON}	Matching delay ON, max(ton)-min(ton), ton are applicable to all 6 driver outputs	-	70	150		external dead time->500ns
MT_{OFF}	Matching delay OFF, max(toff)-min(toff), toff are applicable to all 6 driver outputs	-	90	150		external dead time->500ns
PM	Output pulse width matching. Pw_{in}-PW_{out}		12	100		PW_{in}>1µs

Note 1 : Because of internal signal processing and safety aspects the output H_O at short turn off pulses shows the behaviour according to figure 4. For proper work of the driver the input pulses must not fall below the recommended input width t_{IN} of 1µs.
The short signal range is not subject to production test and is not guaranteed.

4 Timing Diagrams

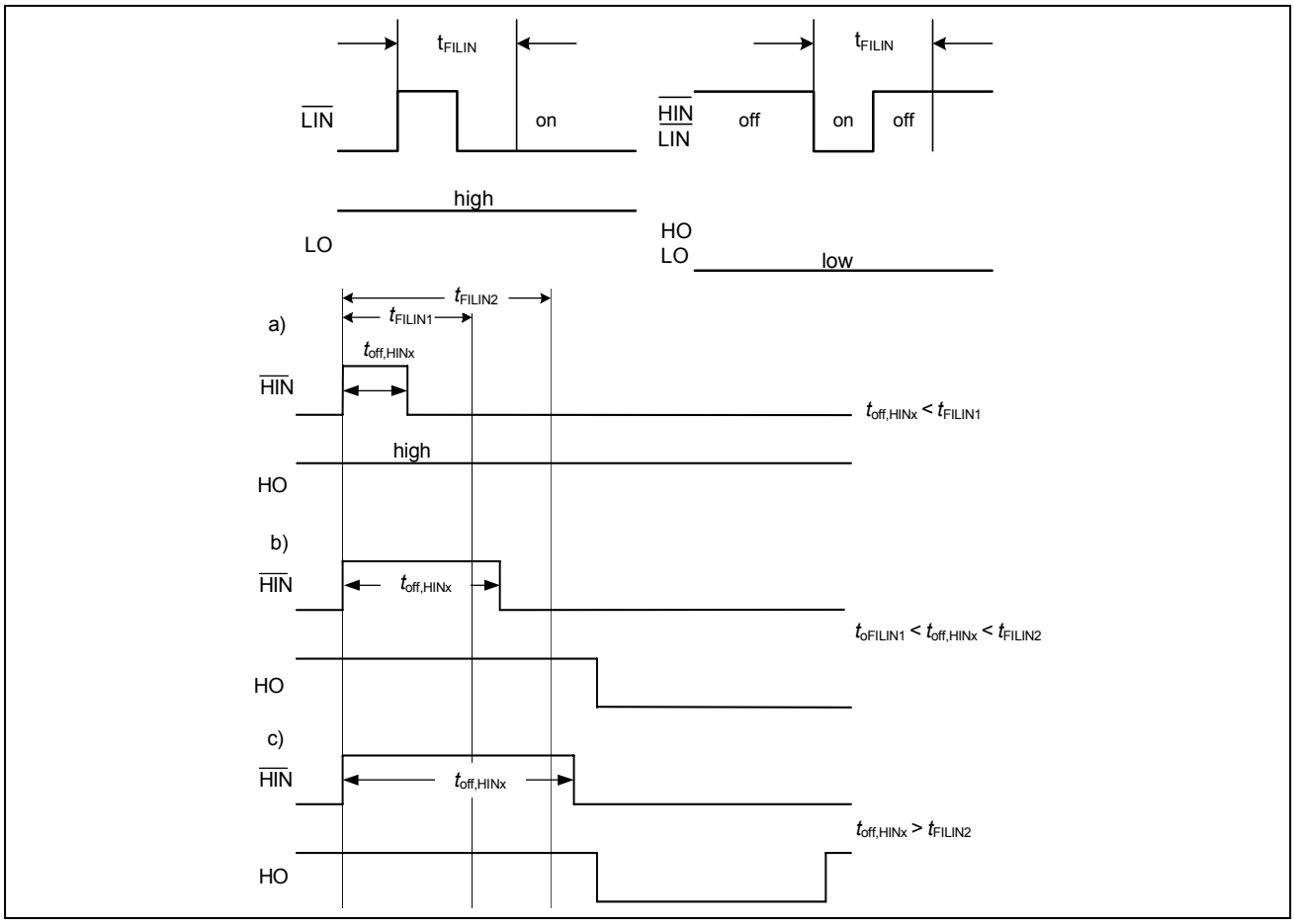


Figure 7: Timing of short pulse suppression

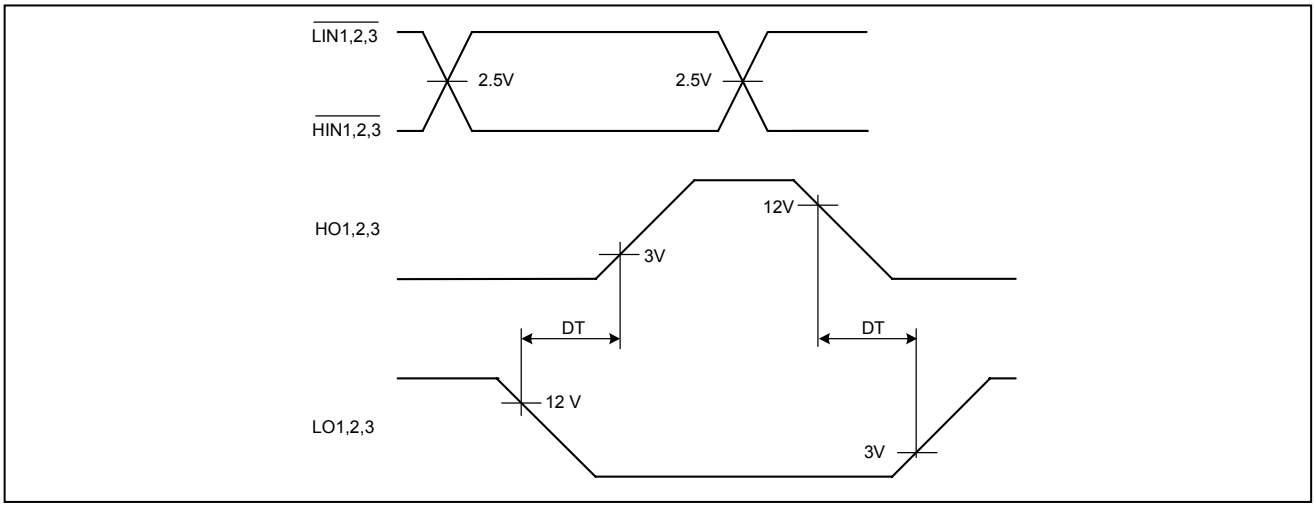


Figure 8: Timing of internal deadtime

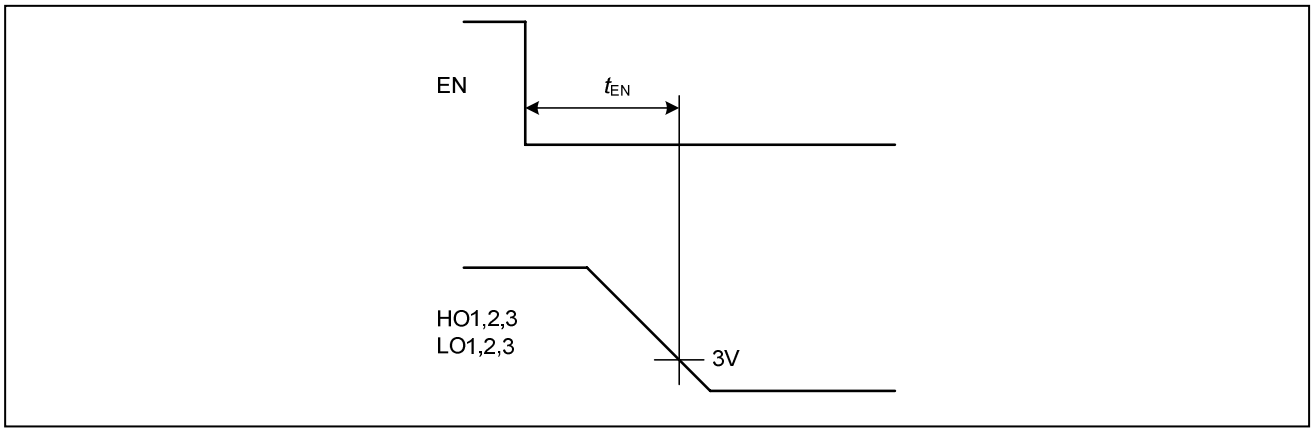


Figure 9: Enable delay time definition

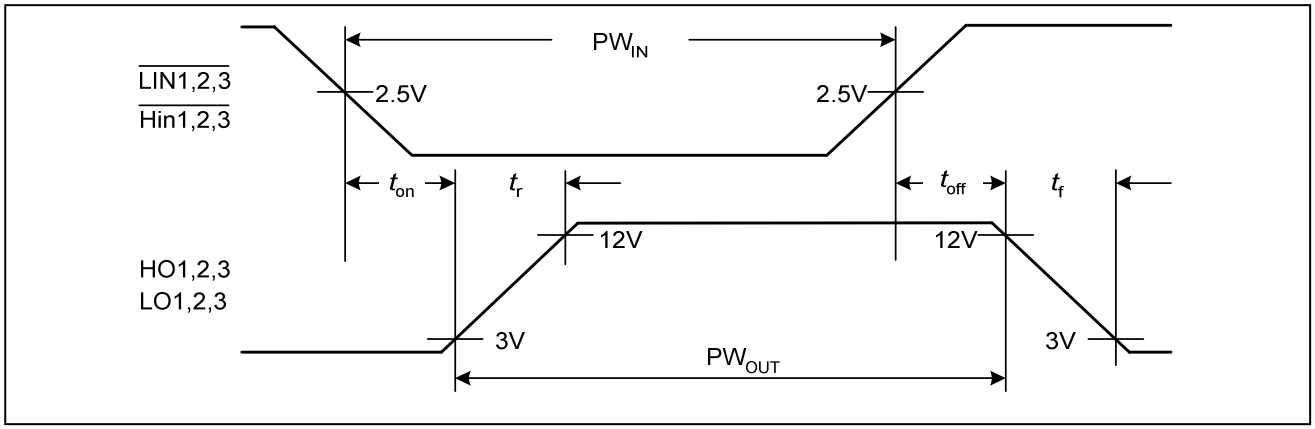


Figure 10: Input to output propagation delay times and switching times definition

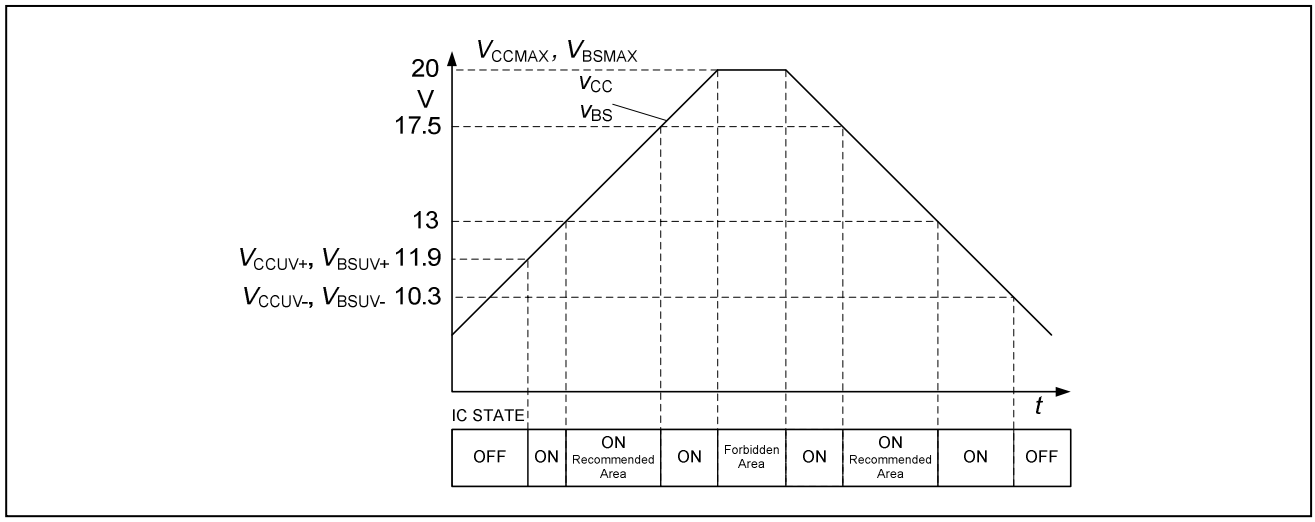


Figure 11: Operating Areas

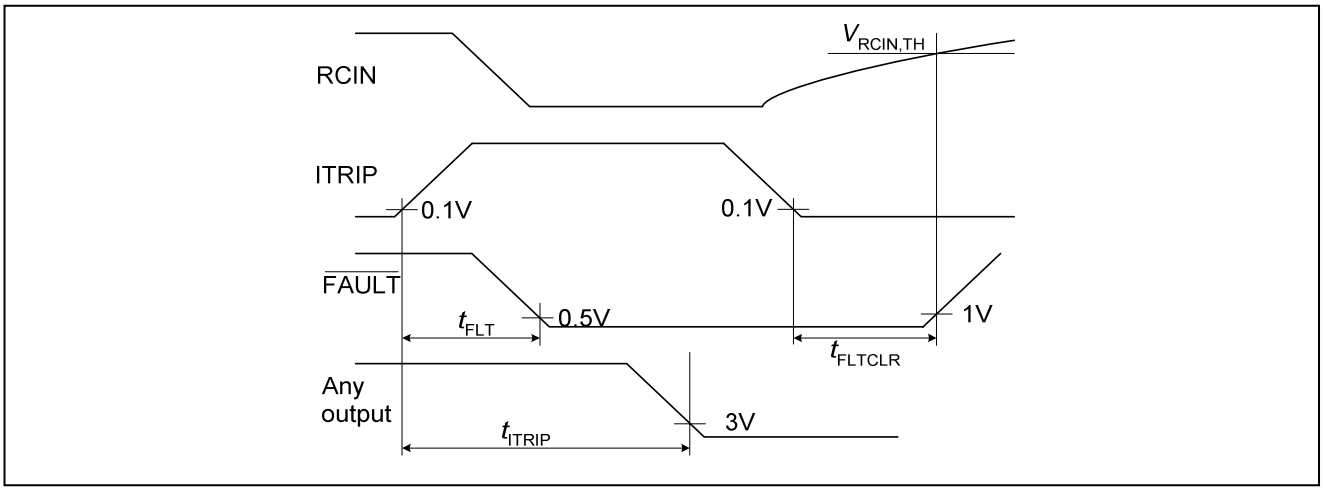
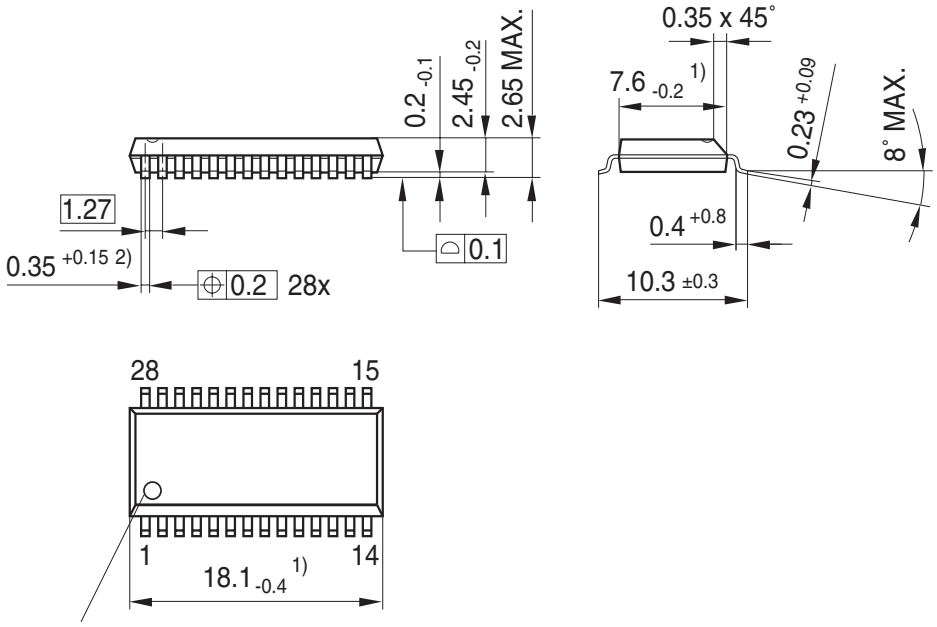


Figure 12: ITRIP-timing

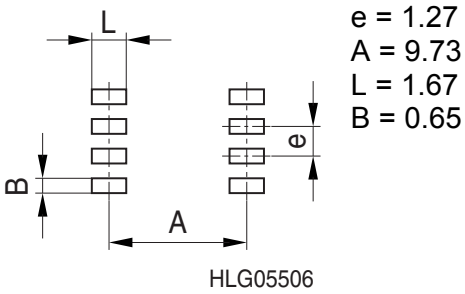
5 Package

5.1 Package Drawing



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

Footprint for Reflow soldering



e = 1.27
A = 9.73
L = 1.67
B = 0.65

5.2 Reference PCB for thermal resistance

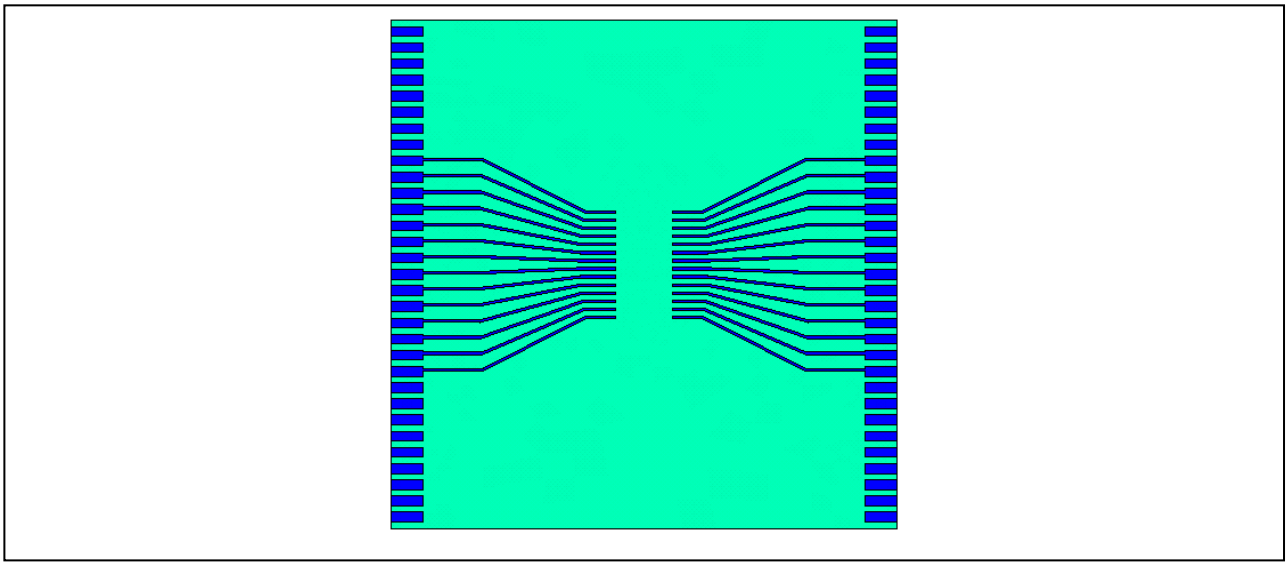


Figure 13: **PCB Reference layout**

Dimensions	80.0 × 80.0 × 1.5 mm³	λ_{therm} [W/m·K]
Material	FR4	0.3
Metal (Copper)	70µm	388